CLOCK GENERATION CIRCUIT AND WIRELESS RECEIVING DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-180088; filed on September 11, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a clock generation circuit and a wireless receiving device.

BACKGROUND

In a wireless receiving device which includes an analog circuit and a digital circuit, harmonics of a clock signal of the digital circuit are introduced into the analog circuit as unnecessary radiation (spurious), and thereby receiving sensitivity is degraded. For this reason, it is preferable that a clock signal to be supplied to a digital circuit is appropriately generated.

Examples of related art include JP-A-2005-191831, JP-A-2001-230765, and JP-A-2004-153637.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram illustrating a configuration of a clock generation circuit according to an embodiment.

FIGS. 2A and 2B are circuit diagrams illustrating a delay unit according to the embodiment.

FIG. 3 is a waveform diagram illustrating an operation of the clock generation circuit according to the embodiment.

FIG. 4 is a diagram illustrating a principle, in which spurious is cancelled, according to the embodiment.

FIG. 5 is a diagram illustrating an operation of the clock generation circuit according to the embodiment.

FIG. 6 is a circuit diagram illustrating a configuration of a wireless receiving device to which the clock generation circuit according to the embodiment is applied.

FIGS. 7A and 7B are diagrams illustrating operations of the wireless receiving device to which the clock generation circuit according to the embodiment is applied.

FIG. 8 is a circuit diagram illustrating a configuration of the clock generation circuit according to a modification example of the embodiment.

FIGS. 9A and 9B are circuit diagrams illustrating configurations of a delay unit according to a modification example of the embodiment.

DETAILED DESCRIPTION

[0004]An object of an embodiment is to provide a clock generation circuit and a wireless receiving device which can appropriately generate a clock signal to be supplied to a digital circuit.

[0005]According to one embodiment, a clock generation circuit including multiple delay lines and a select circuit is provided. The multiple delay line respectively receive input clock signals and provide the amounts of delay different from each other. The select circuit selects one of the multiple delay lines. The select circuit outputs a transferred clock signal through the selected delay line as an output clock signal. The multiple delay lines include a first delay line. The first delay line generates a reference clock signal by providing a first amount of delay to the input clock signal. The multiple delay lines further include at least one of a second delay line and a third delay line. The second delay line provides a second amount of delay to the input clock signal and generates a clock signal that is obtained by advancing edge timing by a fixed amount with respect to the reference clock signal. The second amount of delay is less than the first amount of delay. The third delay line provides a third amount of delay to the input clock signal and generates a clock signal that is obtained by delaying the edge timing by the fixed amount with respect to the reference clock signal. The third amount of delay is greater than the first amount of delay.

[0007]Hereinafter, a clock generation circuit according to the embodiment will be described with reference to the drawings. The invention is not limited to the embodiment.

Embodiment

[0008]A clock generation circuit 1 according to the embodiment is applied to, for example, a wireless receiving device. The wireless receiving device according to wireless standards such as, M-WiMAX, or WLAN and LTE requires high receiving sensitivity in order to secure a wide communication area. In the wireless receiving device, signal processing of a reception signal received in an analog manner is performed in an analog manner by an analog circuit, and signal processing of the signal in which signal processing is performed in an analog manner is performed in a digital manner by a digital circuit. In addition, miniaturization of the wireless receiving device is required, and requirements for one chip LSI of the wireless receiving device in which an analog circuit and a digital circuit are embedded together increase. In the one chip LSI, spurious due to integer harmonics of a clock signal generated by the digital circuit is leaked into an analog circuit, and thereby reception characteristics can be decreased. For this reason, countermeasures for preventing spurious from being generated in an analog circuit can be provided.

[0009]For example, in the wireless receiving device, a digital circuit performs processing of a signal in a digital manner in synchronization with a clock signal generated by the clock generation circuit 1. At this time, if modulation in which edge timing of a clock signal to be generated by the clock generation circuit 1 is randomly changed is performed, spurious can be diffused in a power manner on a frequency spectrum. However, if viewed from a desired frequency band, strength of spurious cannot be reduced to a required level, and thus it is preferable that the strength of the spurious in the desired frequency is further reduced.

[0010]Hence, the embodiment aims to effectively cancel the spurious in a desired frequency band by performing modulation in which a phase of the edge timing of the clock signal to be generated by the clock generation circuit 1 is delayed and/or advanced by a fixed amount corresponding to a desired frequency band.

[0011]Specifically, as illustrated in FIG. 1, the clock generation circuit 1 receives an input clock signal fCKin through an input terminal 2, and generates an output clock signal fCKout by performing modulation in which a phase of the edge timing of the input clock signal fCKin is advanced and/or delayed by a fixed amount Td corresponding to a desired frequency band FBdes. The clock generation circuit 1 outputs the generated output clock signal fCKout from an output terminal 3. FIG. 1 is a diagram illustrating a configuration of the clock generation circuit 1.

[0012]The clock generation circuit 1 performs one selected operation while periodically switching one operation which is selected from a first operation and a second operation with respect to a reference clock signal fCKref (refer to (a) of FIG. 3), and generates the output clock signal. Alternatively, the clock generation circuit 1 performs one selected operation while periodically switching one operation which is selected from the first operation and a third operation with respect to the reference clock signal fCKref, and generates the output clock signal. Alternatively, the clock generation circuit 1 performs one selected operation while periodically switching one operation which is selected from the first operation and the second operation and the third operation with respect to the reference clock signal fCKref, and generates the output clock signal. The first operation includes an operation in which the edge timing of the reference clock signal fCKref is not changed. The second operation includes an operation in which the edge timing of the reference clock signal fCKref advances by the fixed amount Td. The third operation includes an operation in which the edge timing of the reference clock signal fCKref is delayed by the fixed amount Td. For example, the clock generation circuit 1 includes multiple delay lines 10, 20, and 30, a select circuit 40, and a control circuit 50.

[0013]The multiple delay lines 10, 20, and 30 are connected between the input terminal 2 and the select circuit 40. The multiple delay lines 10, 20, and 30 receive the input clock signal fCKin, assign the amount of delay different from each other, and supply the select circuit 40, respectively.

[0014]The delay line 20 generates the reference clock signal fCKref by assigning the amount of delay D1 to the input clock signal fCKin.

[0015]The delay line 30 assigns the amount of delay D2 to the input clock signal fCKin, and generates an advanced-phase clock signal fCK(-) which is obtained by advancing the edge timing by the fixed amount Td with respect to the reference clock signal fCKref. The amount of delay D2 is less than the amount of delay D1 by the fixed amount Td, and is, for example, the amount of delay of zero. At this time, the amount of delay D1 may be equal to the fixed amount Td.

[0016]The delay line 10 assigns the amount of delay D3 to the input clock signal fCKin, and generates a delayed-phase clock signal fCK(+) which is obtained by delaying the edge timing by the fixed amount Td with respect to the reference clock signal fCKref. The amount of delay D3 is more than the amount of delay D1 by the fixed amount Td. At this time, the amount of delay D3 may be equal to 2´(fixed amount Td).

[0017]For example, if amount of delay D1=fixed amount Td, amount of delay D2=0, and amount of delay D3=2´(fixed amount Td), the multiple delay lines 10, 20, and 30 use multiple delay units DE with delay of the fixed amount Td.

[0018]That is, the delay line 10 includes two delay units DE-1 and DE-2. The delay unit DE-1 includes one terminal connected to the input terminal 2 through a node N1, and the other terminal connected to one terminal of the delay unit DE-2. The delay unit DE-2 includes the other terminal connected to an input terminal 40a of the select circuit 40. As a result, the delay line 10 can generate the delayed-phase clock signal fCK(+) by delaying the input clock signal fCKin by amount of delay D3=2´(fixed amount Td), using the two the delay units DE-1 and DE-2.

[0019]The delay line 20 includes one delay unit DE-3. The delay unit DE-3 includes one terminal connected to the input terminal 2 though the node N1, and the other terminal connected to an input terminal 40b of the select circuit 40. As a result, the delay line 20 can generate the delayed-phase clock signal fCKref by delaying the input clock signal fCKin by amount of amount of delay D1=(fixed amount Td), using one delay unit DE-3.

[0020]The delay line 30 does not include a delay unit. The delay line 30 includes one terminal connected to the input terminal 2 through the node N1, and the other terminal connected to an input terminal 40c of the select circuit 40. As a result, the delay line 30 can generate the advanced-phase clock signal fCK(-) without delay the input clock signal fCKin.

[0021]For example, each delay unit DE may be configured such that the amount of delay (for example, the fixed amount Td) is generated by an inverter and an RC circuit, as illustrated in FIG. 2A. FIG. 2A is a circuit diagram illustrating a configuration of the delay unit DE. The delay unit DE illustrated in FIG. 2A includes inverters INV-1 and INV-2, a resistor element R, and a capacitor element C. The inverter INV-1 includes an input side connected to one terminal DEa of the delay unit DE, and an output side connected to one terminal of the resistor element R. The resistor element R includes the other terminal connected to one terminal of the capacitor element C and an input side of the inverter INV-2. The capacitor element C includes the other terminal connected to a ground potential. The inverter INV-2 includes an output side connected to the other terminal Deb of the delay unit DE.

[0022]Alternatively, each delay unit DE may be configured such that the amount of delay (for example, the fixed amount Td) is generated by inverters of n stages (n is even numbers larger than or equal to 2) connected in series, as illustrated in FIG. 2B. FIG. 2B is a circuit diagram illustrating a configuration of the delay unit DE. The delay unit DE illustrated in FIG. 2B includes n inverters INV-1 to INV-n. The inverter INV-1 of a first stage includes an input side connected to the one terminal DEa of the delay unit DE, and an output side connected to an input side of the inverter INV-2 of a second stage. The inverter INV-2 of the second stage includes an output side connected to an input side of an inverter INV-3 of a third stage. An inverter INV-(n-1) of an (n-1)th stage includes an output side connected to an input side of an inverter INV-n of an nth stage. The inverter INV-n of the nth stage includes an output side connected to the other terminal Deb of the delay unit DE.

[0023]Returning to FIG. 1, the select circuit 40 is connected between the multiple delay lines 10, 20, and 30 and the output terminal 3. The select circuit 40 selects one delay line among the multiple delay lines 10, 20, and 30 in accordance with a select signal fA, and outputs a clock signal which is transferred through the selected delay line as an output clock signal fCKout.

[0024]The select circuit 40 includes input terminals 40a to 40c, a control terminal 40d, and an output terminal 40e. The input terminal 40a is connected to an output side of the delay line 10, the input terminal 40b is connected to an output side of the delay line 20, and the input terminal 40c is connected to an output side of the delay line 30. The select circuit 40 receives the delayed-phase clock signal fCK(+) at the input terminal 40a, receives the reference clock signal fCKref at the input terminal 40b, and receives the advanced-phase clock signal fCK(-) at the input terminal 40c.

[0025]The control terminal 40d is connected to the control circuit 50. The select circuit 40 receives the select signal fA with, for example, three values (0 to 2) at the control terminal 40d. If receiving the select signal fA (fA=0) which instructs selecting of the input terminal 40a, the select circuit 40 selects the delayed-phase clock signal fCK(+) to output from an output terminal 40e as the output clock signal fCKout. If receiving the select signal fA (fA=1) which instructs selecting of the input terminal 40b, the select circuit 40 selects the reference clock signal fCKref to output from the output terminal 40e as the output clock signal fCKout. If receiving the select signal fA (fA=2) which instructs selecting of the input terminal 40c, the select circuit 40 selects the advanced-phase clock signal fCK(-) to output from the output terminal 40e as the output clock signal fCKout.

[0026]The control circuit 50 controls the select circuit 40 by receiving a control signal fCS from the outside (for example, a digital circuit 170 illustrated in FIG. 6), generating the select signal fA based on the control signal fCS, and supplying the select signal fA to the select circuit 40. That is, the control circuit 50 controls the select circuit 40 such that the selected one operation is performed while one operation which is selected from the first operation and the second operation is periodically switched, with respect to the reference clock signal fCKref. Alternatively, the clock generation circuit 1 controls the select circuit 40 such that the selected one operation is performed while one operation which is selected from the first operation and the third operation is periodically switched, with respect to the reference clock signal fCKref. Alternatively, the clock generation circuit 1 controls the select circuit 40 such that the selected one operation is performed while one operation which is selected from the first operation, the second operation, and the third operation is periodically switched, with respect to the reference clock signal fCKref. The first operation includes an operation in which the edge timing of the reference clock signal fCKref is not changed. The second operation includes an operation in which the edge timing of the reference clock signal fCKref is advanced by the fixed amount Td. The third operation includes an operation in which the edge timing of the reference clock signal fCKref is delayed by the fixed amount Td.

[0027]For example, if a waveform of the reference clock signal fCKref is a waveform illustrated in (a) of FIG. 3, the control circuit 50 controls the select circuit 40 such that the selected one operation is performed while one operation which is selected from the first operation and the second operation is periodically switched, with respect to the reference clock signal fCKref, as illustrated in (b) of FIG. 3. FIG. 3 is a waveform diagram illustrating an operation of the clock generation circuit.

[0028]That is, at timing t0, the control circuit 50 has the select signal fA=1.

[0029]At timing t01, the control circuit 50 changes the select signal from the select signal fA=1 to the select signal fA=2. According to this, the select circuit 40 is switched from a state in which the reference clock signal fCKref is selected to a state in which the advanced-phase clock signal fCK(-) is selected, and thus a falling edge of a clock signal fCKscc1 is advanced by the fixed amount Td from timing t1.

[0030]At timing t12, the control circuit 50 changes the select signal from the select signal fA=2 to the select signal fA=1. According to this, the select circuit 40 returns to a state in which the reference clock signal fCKref is selected from a state in which the advanced-phase clock signal fCK(-) is selected, and thus a rising edge of the clock signal fCKscc1 becomes the same as that of the reference clock signal fCKref at timing t2.

[0031]The control circuit 50 controls the select circuit 40 such that the select circuit 40 also repeats the same operation as at a clock period TP1 at other clock periods TP2 to TP4. Timings t01 and t12 are respectively earlier than timings t1 and t2 of the reference clock signal fCKref by time according to the fixed amount Td and operation time of the select circuit 40.

[0032]Alternatively, as illustrated in (c) of FIG. 3, the control circuit 50 controls the select circuit 40 such that the selected one operation is performed while one operation which is selected from the first operation and the third operation is periodically switched, with respect to the reference clock signal fCKref.

[0033]That is, at timing t0, the control circuit 50 has the select signal fA=1.

[0034]At timing t01, the control circuit 50 changes the select signal from the select signal fA=1 to the select signal fA=0. According to this, the select circuit 40 is switched from a state in which the reference clock signal fCKref is selected to a state in which the delayed-phase clock signal fCK(+) is selected, and thus a falling edge of a clock signal fCKscc2 is delayed by the fixed amount Td from timing t1.

[0035]At timing t12, the control circuit 50 changes the select signal from the select signal fA=0 to the select signal fA=1. According to this, the select circuit 40 returns to a state in which the reference clock signal fCKref is selected from a state in which the delayed-phase clock signal fCK(+) is selected, and thus a rising edge of the clock signal fCKscc2 becomes the same as that of the reference clock signal fCKref at timing t2.

[0036]The control circuit 50 controls the select circuit 40 such that the select circuit 40 also repeats the same operation as at a clock period TP1 at other clock periods TP2 to TP4. Timings t01 and t12 are respectively earlier than timings t1 and t2 of the reference clock signal fCKref by the time according to the fixed amount Td and operation time of the select circuit 40.

[0037] Alternatively, as illustrated in (d) of FIG. 3, the control circuit 50 controls the select circuit 40 such that the selected one operation is performed while one operation which is selected from the first operation, the second operation, and the third operation is periodically switched, with respect to the reference clock signal fCKref.

[0038]That is, at timing t0, the control circuit 50 has the select signal fA=1.

[0039]At timing t01, the control circuit 50 changes the select signal from the select signal fA=1 to the select signal fA=2. According to this, the select circuit 40 is switched from a state in which the reference clock signal fCKref is selected to a state in which the advanced-phase clock signal fCK(-) is selected, and thus a falling edge of a clock signal fCKscc3 is advanced by the fixed amount Td from timing t1.

[0040]At timing t12, the control circuit 50 changes the select signal from the select signal fA=2 to the select signal fA=1. According to this, the select circuit 40 returns to a state in which the reference clock signal fCKref is selected from a state in which the advanced-phase clock signal fCK(-) is selected, and thus a rising edge of the clock signal fCKscc3 becomes the same as that of the reference clock signal fCKref at timing t2.

[0041]At timing t23, the control circuit 50 changes the select signal from the select signal fA=1 to the select signal fA=0. According to this, the select circuit 40 is switched from a state in which the reference clock signal fCKref is selected to a state in which the delayed-phase clock signal fCK(+) is selected, and thus the falling edge of the clock signal fCKscc3 is delayed by the fixed amount Td from timing t3.

[0042]At timing t34, the control circuit 50 changes the select signal from the select signal fA=0 to the select signal fA=1. According to this, the select circuit 40 returns to a state in which the reference clock signal fCKref is selected from a state in which the delayed-phase clock signal fCK(+) is selected, and thus the rising edge of the clock signal fCKscc3 becomes the same as that of the reference clock signal fCKref at timing t4.

[0043]The control circuit 50 controls the select circuit 40 such that the select circuit 40 also repeats the same operation as at a set of clock periods TP1 and TP2 at other clock periods TP3 and TP4. Timings t01, t12, t23, and t34 are respectively earlier than timings t1, t2, t3, and t4 of the reference clock signal fCKref by the time according to the fixed amount Td and operation time of the select circuit 40.

[0044]Alternatively, as illustrated in (e) of FIG. 3, the control circuit 50 controls the select circuit 40 such that the selected one operation is performed while one operation which is selected from the first operation and the second operation is periodically switched, with respect to the reference clock signal fCKref.

[0045]That is, at timing t0, the control circuit 50 has the select signal fA=1.

[0046]At timing t12, the control circuit 50 changes the select signal from the select signal fA=1 to the select signal fA=2. According to this, the select circuit 40 is switched from a state in which the reference clock signal fCKref is selected to a state in which the advanced-phase clock signal fCK(-) is selected, and thus a falling edge of a clock signal fCKscc4 is delayed by the fixed amount Td from timing t2.

[0047]At timing t23, the control circuit 50 maintains the select signal fA=2. According to this, the select circuit 40 maintains a state in which the advanced-phase clock signal fCK(-) is selected, and thus the falling edge of the clock signal fCKscc4 is advanced by the fixed amount Td from timing t3.

[0048]At timing t34, the control circuit 50 changes the select signal from the select signal fA=2 to the select signal fA=1. According to this, the select circuit 40 returns to a state in which the reference clock signal fCKref is selected from a state in which the advanced-phase clock signal fCK(-) is selected, and thus a rising edge of the clock signal fCKscc4 becomes the same as that of the reference clock signal fCKref at timing t4.

[0049]The control circuit 50 controls the select circuit 40 such that the select circuit 40 also repeats the same operation as at a set of clock periods TP1 and TP2 at other clock periods TP3 and TP4. Timings t01, t12, t23, and t34 are respectively earlier than timings t1, t2, t3, and t4 of the reference clock signal fCKref by the time according to the fixed amount Td and operation time of the select circuit 40.

[0050]Alternatively, as illustrated in (f) of FIG. 3, the control circuit 50 controls the select circuit 40 such that the selected one operation is performed while one operation which is selected from the first operation and the third operation is periodically switched, with respect to the reference clock signal fCKref.

[0051]That is, at timing t0, the control circuit 50 has the select signal fA=1.

[0052]At timing t12, the control circuit 50 changes the select signal from the select signal fA=1 to the select signal fA=0. According to this, the select circuit 40 is switched from a state in which the reference clock signal fCKref is selected to a state in which the delayed-phase clock signal fCK(+) is selected, and thus a rising edge of a clock signal fCKscc5 is delayed by the fixed amount Td from timing t2.

[0053]At timing t23, the control circuit 50 maintains the select signal fA=0. According to this, the select circuit 40 maintains a state in which the delayed-phase clock signal fCK(+) is selected, and thus a falling edge of the clock signal fCKscc5 is advanced by the fixed amount Td from timing t3.

[0054]At timing t34, the control circuit 50 changes the select signal from the select signal fA=0 to the select signal fA=1. According to this, the select circuit 40 returns to a state in which the reference clock signal fCKref is selected from a state in which the delayed-phase clock signal fCK(+) is selected, and thus the rising edge of the clock signal fCKscc5 becomes the same as that of the reference clock signal fCKref at timing t4.

[0055]The control circuit 50 controls the select circuit 40 such that the select circuit 40 also repeats the same operation as at a set of clock periods TP1 and TP2 at other clock periods TP3 and TP4. Timings t01, t12, t23, and t34 are respectively earlier than timings t1, t2, t3, and t4 of the reference clock signal fCKref by the time according to the fixed amount Td and operation time of the select circuit 40.

[0056]Alternatively, as illustrated in (g) of FIG. 3, the control circuit 50 controls the select circuit 40 such that the selected one operation is performed while one operation which is selected from the first operation, the second operation, and the third operation is periodically switched, with respect to the reference clock signal fCKref.

[0057]That is, at timing t0, the control circuit 50 has the select signal fA=1.

[0058]At timing t12, the control circuit 50 changes the select signal from the select signal fA=1 to the select signal fA=2. According to this, the select circuit 40 is switched from a state in which the reference clock signal fCKref is selected to a state in which the advanced-phase clock signal fCK(-) is selected, and thus a rising edge of a clock signal fCKscc6 is delayed by the fixed amount Td from timing t2.

[0059]At timing t23, the control circuit 50 maintains the select signal fA=2. According to this, the select circuit 40 maintains a state in which the advanced-phase clock signal fCK(-) is selected, and thus a falling edge of the clock signal fCKscc6 is advanced by the fixed amount Td from timing t3.

[0060]At timing t34, the control circuit 50 changes the select signal from the select signal fA=2 to the select signal fA=1. According to this, the select circuit 40 returns to a state in which the reference clock signal fCKref is selected from a state in which the advanced-phase clock signal fCK(-) is selected, and thus the rising edge of the clock signal fCKscc6 becomes the same as that of the reference clock signal fCKref at timing t4.

[0061]At timing t56, the control circuit 50 changes the select signal from the select signal fA=1 to the select signal fA=0. According to this, the select circuit 40 returns to a state in which the reference clock signal fCKref is selected from a state in which the delayed-phase clock signal fCK(+) is selected, and thus the rising edge of the clock signal fCKscc6 becomes the same as that of the reference clock signal fCKref at timing t6.

[0062]At timing t67, the control circuit 50 maintains the select signal fA=0. According to this, the select circuit 40 maintains a state in which the delayed-phase clock signal fCK(+) is selected, and thus the falling edge of the clock signal fCKscc6 is delayed by the fixed amount Td from timing t7.

[0063]At timing t78, the control circuit 50 changes the select signal from the select signal fA=0 to the select signal fA=1. According to this, the select circuit 40 returns to a state in which the reference clock signal fCKref is selected from a state in which the delayed-phase clock signal fCK(+) is selected, and thus the rising edge of the clock signal fCKscc6 becomes the same as that of the reference clock signal fCKref at timing t8.

[0064]The control circuit 50 controls the select circuit 40 such that the select circuit 40 also repeats the same operation as at a set of clock periods TP1 to TP4 at other sets of clock periods. Timings t01, t12, t23, t34, t56, t67, and t78 are respectively earlier than timings t1, t2, t3, t4, t6, t7, and t8 of the reference clock signal fCKref by the time according to the fixed amount Td and operation time of the select circuit 40.

[0065]Subsequently, a principle in which spurious is cancelled will be described, using FIG. 4. Fig. 4 is a diagram illustrating a principle in which spurious is cancelled. FIG. 4 illustrates the principle in which spurious is cancelled, with reference to the clock signal fCKscc1 illustrated in (b) of FIG. 3.

[0066]It is considered that propagation of spurious is caused by a current (@voltage) flowing into Vdd/Vss in accordance with a clock signal rather than the clock signal itself. For this reason, description will be made by separating a spurious current into a current originated from a rising edge and a current originated from a falling edge.

[0067]For example, a waveform of the clock signal fCKscc1 includes rising edge components illustrated in (a) of FIG. 4, and falling edge components illustrated in (b) of FIG. 4. Among these, the rising edge components are the same as those of the reference clock signal fCKref (refer to (a) of FIG. 3), but the falling edge components advance from the falling edge of the reference clock signal fCKref by the fixed amount Td. That is, in (b) of FIG. 4, dashed lines denote falling edges of the reference clock signal fCKref, and solid lines denote falling edges of the clock signal fCKscc1. Arrows of (b) of FIG. 4 represent that the falling edges (dashed lines) of the reference clock signal fCKref advance by the fixed amount Td, and thereby the falling edges (solid lines) of the clock signal fCKscc1 are generated.

[0068]Behavior of the components of the rising edge illustrated in (a) of FIG. 4 can be approximately represented by a sine wave WF1 with periods equivalent to and amplitudes corresponding rising edges illustrated in (c) of FIG. 4. Behavior of the components of the falling edge illustrated in (b) of FIG. 4 can be approximately represented by a sine wave WF2 with periods equivalent to and amplitudes corresponding to falling edges denoted by a solid line of (d) of FIG. 4. That is, in (d) of FIG. 4, a dashed line illustrates a sine wave WF2’ with periods equivalent to and amplitudes corresponding to falling edges of the reference clock signal fCKref, a solid line illustrates a sine wave WF2 with periods equivalent to and amplitudes corresponding to falling edges of the clock signal fCKscc1. An arrow of (d) of FIG. 4 represents that a phase of the sine wave WF2’ (dashed line) advances by the fixed amount Td and thereby the sine wave WF2 (solid line) is generated.

[0069]In addition, behavior of spurious components generated from component of the rising edge illustrated in (a) of FIG. 4 can be approximately represented by a sine wave WF10 with a frequency that is M times (M is even numbers larger than or equal to 2 and M=10 in FIG. 4) the frequency of the sine wave WF1 as illustrated in (e) of FIG. 4. In the same manner, behavior of spurious components generated from component of the falling edge illustrated in (b) of FIG. 4 can be approximately represented by a sine wave WF20 with a frequency that is M times the frequency of the sine wave WF2 as denoted by a solid line of (f) of FIG. 4. That is, in (f) of FIG. 4, the solid line denotes the sine wave WF20’ with a frequency that is M times the frequency of the sine wave WF2’, and denotes the sine wave WF20 with a frequency that is M times the frequency of the sine wave WF2. Arrows of (f) of FIG. 4 represent that a phase of the sine wave WF20’ (dashed line) advances by the fixed amount Td and thereby the sine wave WF20 (solid line) is generated.

[0070]As illustrated in (e) and (f) of FIG. 4, the sine waves WF10 and WF20’ have approximately the same phase as each other. For this reason, if the sine waves WF10 and WF20’ are synthesized with each other, spurious components are reinforced with each other, as denoted by a dashed line of (g) of FIG. 4. Meanwhile, as denoted by dashed lines of (e) and (f) of FIG. 4, the sine waves WF10 and WF20 have approximately reverse phases (a phase difference between a rising edge and a falling edge is 180 degrees) each other. For this reason, if the sine waves WF10 and WF20 are synthesized with each other, the spurious components can be cancelled with each other, as denoted by a dashed line of (g) of FIG. 4.

[0071]In FIG. 3, when the output clock signals are generated, a case in which one of the second operation and the third operation is performed in addition to the first operation (refer to (b), (c), (e), and (f) of FIG. 3), and a case in which the second operation and the third operation are alternately performed in addition to the first operation (refer to (d) and (g) of FIG. 3) are illustrated. The first operation includes an operation in which edge timing of the reference clock signal fCKref is not changed. The second operation includes an operation in which the edge timing of the reference clock signal fCKref advances by the fixed amount Td. The third operation includes an operation in which the edge timing of the reference clock signal fCKref is delayed by the fixed amount Td. The amount of shift of edge timing of each of the second operation and the third operation is set to the fixed amount Td, but may be varied due to the effect of variation or the like of operation characteristics of the delay unit DE in the actual operation. In contrast to this, if a case in which one of the second operation and the third operation is performed is compared with a case in which the second operation and the third operation are alternately performed, it can be seen that a case in which the second operation and the third operation are alternately performed is strong against variation of the amount of shift of the edge timing. This point will be hereinafter described by using expressions.

[0072]When a clock signal is generated by performing one of the second operation and the third operation for the reference clock signal fCKref in addition to the first operation, a signal with spurious components of a predetermined frequency of the reference clock signal fCKref is summed with a signal obtained by advancing (or delaying) the edge of the reference clock signal fCKref, and thereby spurious components of the predetermined frequency are cancelled. When a phase of spurious components of a predetermined frequency is referred to as q, a phase difference (phase difference denoted by a unit of a phase (phase angle) with respect to one period of the spurious components of the predetermined frequency) corresponding to the amount of shift of the edge timing of the clock signal is referred to as f, and amplitude without phase shift (f=0) is 1, the expression of the summed signal is as follows.

f2waves(q,f)=1/2´sinq+1/2´sin(q+f)¼Expression 1.

[0073]Expression 1 is organized as the following Expression 2 to Expression 4.

f2waves(q,f)=Ö[(1+cosf)/2]´sin(q+a)¼Expression 2,

When -90°£f<90°, a=tan-1[sinf/(1+cosf)]+0¼Expression 3,

When 90°£f<270°, a=tan-1[sinf/(1+cosf)]+p¼Expression 4.

[0074]According to Expression 2 to Expression 4, amplitude of the synthesized signal is represented by the following Expression 5.

Amp2=Ö[(1+cosf)/2]¼Expression 5.

[0075]Meanwhile, when a clock signal is generated by alternately performing (that is, performing both) the second operation and the third operation for the reference clock signal fCKref in addition to the first operation, a signal with spurious components of a predetermined frequency of the reference clock signal fCKref, a signal obtained by advancing the edge of the reference clock signal fCKref, and a signal obtained by delaying the edge of the reference clock signal fCKref are summed together, and thereby spurious components of the predetermined frequency are cancelled. When a phase of the reference clock signal fCKref is referred to as q, a phase difference between a phase of the reference clock signal fCKref and a phase of an advanced (or delayed) clock signal is referred to as f, and amplitude without phase shift (f=0) is 1, the expression of the summed signal (synthesized signal) is as the following Expression 6.

f4waves(q,f)=1/2´sinq+1/2´sin(q+f)+1/2´sinq+1/2´(q-f)¼Expression 6.

[0076]Expression 6 is organized as the following Expression 7.

f4waves(q,f)=[(1+cosf)/2]´sinq¼Expression 7.

[0077]According to Expression 7, amplitude of the synthesized signal is represented by the following Expression 8.

Amp4=Ö[(1+cosf)/2]¼Expression 8.

[0078]FIG. 5 is obtained by plotting the phase difference f corresponding to the amount of shift of the edge timing of the clock signal and the removed amount of the spurious, using Expression 5 (one) and Expression 8 (alternating). FIG. 5 is a diagram illustrating an operation of the clock generation circuit 1. It can be seen from FIG. 5 that, also in both of a case in which one of the second operation and the third operation is performed for the reference clock signal fCKref in addition to the first operation, and a case in which the second operation and the third operation are alternately (that is, both) performed, when the phase difference corresponding to the amount of shift of the edge timing of the clock signal is 180 degrees, the amount of attenuation of the spurious is maximum.

[0079]For example, if a frequency that a user want to cancel the spurious is referred to as fspur, a relationship of following Expression 9 is satisfied between a phase difference f corresponding to the amount of shift of the edge timing of the clock signal and the amount of shift, that is, the fixed amount Td obtained by advancing or delaying a rising/falling edge.

f=Td´fspur´360°¼Expression 9

[0080]Following Expression 10 is obtained by inserting f=180° into Expression 9 to calculate Td.

Td=1/(2fspur)¼Expression 10

[0081]In FIG. 5, it can be seen that the spurious components can be efficiently cancelled in a case in which the clock signal is generated by alternately performing the second operation and the third operation (for example, a case of (d) and (g) of FIG. 3), compared to a case in which the clock signal is generated by performing one of the second operation and the third operation for the reference clock signal fCKref in addition to the first operation (for example, a case of (b), (c), (e), (f) of FIG. 3).

[0082]Subsequently, a wireless receiving device 100 to which the clock generation circuit 1 is applied will be described with reference to FIG. 6. FIG. 6 is a diagram illustrating a configuration of the wireless receiving device 100.

[0083]The wireless receiving device 100 includes an antenna AT, an analog circuit 160, a digital circuit 170, an original oscillator XO, a local oscillation circuit SYN, and clock generation circuits 1-1 and 1-2. The analog circuit 160 includes a low noise antenna LNA, a mixer MIX, a low pass filter LOW PASS FILTER, and a variable amplifier AMP. The digital circuit 170 includes an AD converter ADC and a digital processing circuit DPC. In the wireless receiving device 100, the clock generation circuits 1-1 and 1-2 are respectively provided with respect to the AD converter ADC and the digital processing circuit DPC, and are configured such that operations of modulating the clock signal can be on/off separately from each other.

[0084]In the wireless receiving device 100, if clock modulation operations of the clock generation circuits 1-1 and 1-2 are off, spurious components denoted by arrows of FIG. 7A can be generated. In contrast to this, if clock modulation operations are on, spurious components denoted by arrows of FIG. 7B can be generated. FIG.s 7A and 7B are respectively diagram illustrating an operation of the wireless receiving device 100, a vertical axis denotes power, and a horizontal axis denotes a frequency. When the clock modulation operation is on (FIG. 7B), unnecessary spurious components are newly generated in a frequency which is not generated when the clock modulation operation is off (FIG. 7A). For this reason, a function of making the clock modulation operations of the clock generation circuits 1-1 and 1-2 on/off is effective according to the frequency bands to be used.

[0085]For example, if a receiving channel is a signal denoted by a one-dotted chain line of FIG. 7A, a frequency with the spurious components denoted by arrows does not overlap a frequency of a desired signal. FIGS. 7A and 7B are diagrams illustrating an operation of the wireless receiving device 100. For this reason, the digital processing circuit DPC controls the clock generation circuits 1-1 and 1-2 such that the clock modulations performed by the clock generation circuits 1-1 and 1-2 are off. The clock generation circuits 1-1 and 1-2 continuously output the reference clock signal fCKref (refer to (a) of FIG. 3). Meanwhile, if a receiving channel is a signal denoted by a dashed line of FIG. 7B, the frequency with the spurious components denoted by the arrows overlaps a frequency of a desired signal. For this reason, the digital processing circuit DPC controls the clock generation circuits 1-1 and 1-2 such that the clock modulations performed by the clock generation circuits 1-1 and 1-2 are on. The clock generation circuits 1-1 and 1-2 output clock signals (refer to (b) to (g) of FIG. 3) obtained by modulating the reference clock signal fCKref.

[0086]Alternatively, for example, if a signal level is high and the effect of spurious on a receiving signal decreases, necessity for modulating the clock signal decreases. For this reason, the digital processing circuit DPC controls the clock generation circuits 1-1 and 1-2 such that the clock modulations performed by the clock generation circuits 1-1 and 1-2 are off. The clock generation circuits 1-1 and 1-2 continuously output the reference clock signal fCKref (refer to (a) of FIG. 3). Meanwhile, if a signal level is low and the effect of spurious on a receiving signal decreases, necessity for modulating the clock signal increases. For this reason, the digital processing circuit DPC controls the clock generation circuits 1-1 and 1-2 such that the clock modulations performed by the clock generation circuits 1-1 and 1-2 are on. The clock generation circuits 1-1 and 1-2 output clock signals (refer to (b) to (g) of FIG. 3) obtained by modulating the reference clock signal fCKref.

[0087]As described above, in the embodiment, modulation is performed in which a phase of the edge timing of the clock signal to be generated by the clock generation circuit 1 is advanced and/or delayed by the fixed amount Td (for example, 1/(2fspur)) corresponding to a desired frequency fspur with respect to the reference clock signal fCKref. As a result, it is possible to effectively cancel the spurious of a band of a desired frequency.

[0088]The clock generation circuit 1 may have a configuration in which, if one of advancing and delaying a phase by the fixed amount Td with respect to the reference clock signal fCKref is performed, an unused delay line among the multiple delay lines 10 to 30 is omitted. For example, if the clock signal fCKscc1 illustrated in (b) of FIG. 3 or the clock signal fCKscc4 illustrated in (e) of FIG. 3 is generated as the output clock signal fCKout, the clock generation circuit 1 may have a configuration in which the delay line 10 is omitted. Alternatively, if the clock signal fCKscc1 illustrated in (c) of FIG. 3 or the clock signal fCKscc4 illustrated in (f) of FIG. 3 is generated as the output clock signal fCKout, the clock generation circuit 1 may have a configuration in which the delay line 30 is omitted.

[0089]Alternatively, in a clock generation circuit 1i, the amount of delay of each delay unit DEi may vary by considering manufacturing variation of each delay unit DEi, as illustrated in FIG. 8. FIG. 8 is a circuit diagram illustrating a configuration of the clock generation circuit 1i. For example, if the amount of delay of the delay units DEi-1 to DEi-3 is shifted from the fixed amount Td, the amount of delay of the delay units DEi-1 to DEi-3 is changed so as to match the amount of delay corresponding to the fixed amount Td.

[0090]For example, as illustrated in FIG. 9A, each delay unit DEi may have a configuration in which the resistor element R and the capacitor element C are respectively replaced with a variable resistor element Ri and a variable capacitor element Ci, with respect to a configuration illustrated in FIG. 2A. FIGS. 9A and 9B are circuit diagrams illustrating configurations of a delay unit Dei.

[0091]Alternatively, as illustrated in FIG. 9B, each delay unit Dei may have a configuration in which a switching circuit SW that switches the number of stages of inverters to be passed through between one terminal DEa and the other terminal DEb is provided between the one terminal DEa and the inverters of n stages, with respect to a configuration illustrated in FIG. 2B.

[0092]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A clock generation circuit comprising:

multiple delay lines which respectively receive input clock signals and provide amounts of delay different from each other; and

a select circuit which selects one of the multiple delay lines, and outputs a transferred clock signal through a selected delay line as an output clock signal,

wherein the multiple delay lines include a first delay line which provides a first amount of delay to the input clock signal and generates a reference clock signal, and

wherein the multiple delay lines further include at least one of a second delay line which provides a second amount of delay less than the first amount of delay to the input clock signal and generates a clock signal that is obtained by advancing edge timing by a fixed amount with respect to the reference clock signal, and a third delay line which provides a third amount of delay greater than the first amount of delay to the input clock signal and generates a clock signal that is obtained by delaying the edge timing by the fixed amount with respect to the reference clock signal.

2. The circuit according to Claim 1,

wherein the first delay line includes two delay units,

wherein the second delay line includes one delay unit,

and

wherein the third delay line does not include a delay unit.

3. The circuit according to Claim 1 or 2, further comprising:

a control circuit which controls the select circuit such that the output clock signal is generated by performing selected one operation, while one operation is periodically switched which is selected from a first operation in which edge timing is not changed with respect to the reference clock signal, and a second operation in which edge timing is advanced by a fixed amount with respect to the reference clock signal, or the output clock signal is generated by performing selected one operation, while one operation is periodically switched which is selected from the first operation and a third operation in which edge timing is delayed by the fixed amount, or the output clock signal is generated by performing selected one operation, while one operation is periodically switched which is selected from the first operation, the second operation, and the third operation.

4. The circuit according to any one of Claims 1 to 3, wherein the fixed amount corresponds to 1/(2fspur), when a desired frequency which will suppress spurious is referred to as fspur.

5. A clock generation circuit performing

generation of an output clock signal by performing selected one operation, while one operation is periodically switched which is selected from a first operation in which edge timing is not changed with respect to the reference clock signal, and a second operation in which edge timing is advanced by a fixed amount with respect to the reference clock signal, or

generation of the output clock signal by performing selected one operation, while one operation is periodically switched which is selected from the first operation and a third operation in which edge timing is delayed by the fixed amount, or

generation of the output clock signal by performing selected one operation, while the one operation is periodically switched which is selected from the first operation, the second operation, and the third operation.

6. A wireless receiving device comprising:

the clock generation circuit according to any one of Claims 1 to 5; and

a digital circuit which receives an output clock signal that is generated by the clock generation circuit.

ABSTRACT

According to one embodiment, a clock generation circuit including multiple delay lines and a select circuit is provided. The multiple delay line respectively receive input clock signals and provide amounts of delay different from each other. The select circuit selects one of the multiple delay lines. The select circuit outputs a transferred clock signal through a selected delay line as an output clock signal. The multiple delay lines include a first delay line. The first delay line generates a reference clock signal by providing a first amount of delay to the input clock signal. The multiple delay lines further include at least one of a second delay line and a third delay line. The second delay line provides a second amount of delay to the input clock signal and generates a clock signal that is obtained by advancing edge timing by a fixed amount with respect to the reference clock signal. The second amount of delay is less than the first amount of delay. The third delay line provides a third amount of delay to the input clock signal and generates a clock signal that is obtained by delaying the edge timing by the fixed amount with respect to the reference clock signal. The third amount of delay is greater than the first amount of delay.

Drawings

FIG. 1

50: CONTROL CIRCUIT

FIG. 3

ADVANCE

DELAY

FIG. 4

(a) RISING EDGE OF WAVEFORM OF fCKscc1

(b) FALLING EDGE OF WAVEFORM OF fCKscc1

(c) SINE WAVE WF1 HAVING PERIOD EQUIVALENT TO RISING EDGE

(d) SINE WAVE WF2 HAVING PERIOD EQUIVALENT TO FALLING EDGE

(e) SINE WAVE WF10 WHOSE FREQUENCY IS M TIMES FREQUENCY OF SINE WAVE WF1

(f) SINE WAVE WF20 WHOSE FREQUENCY IS M TIMES FREQUENCY OF SINE WAVE WF2

(g)WF10+WF20

FIG. 5

LARGE¬REMOVED AMOUNT OF SPURIOUS®SMALL

PHASE DIFFERENCE f[deg] CORRESPONDING TO AMOUNT OF SHIFT OF EDGE TIMING OF CLOCK SIGNAL

··· ONE SIDE

¾ ALTERNATING

FIG. 6

160: ANALOG CIRCUIT

170: DIGITAL CIRCUIT

FIG. 8

CONTROL CIRCUIT